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PATENT APPLICATION

ATTORNEY DOCKET NO. 200300353-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Roy M. Zeighami et al. Confirmation No.: 4318

Application No.: 10/725,720 Examiner: M.R. Wallis

Filing Date: 12/02/2003 Group Art Unit: 2836

Title: POWER SUPPLY SYSTEM

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 6/19/2007.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $450	☐ 3rd Month $1020	☐ 4th Month $1590

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

Roy M. Zeighami et al.

By: 
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Docket No.: 200300353-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Roy M. Zeighami et al.
Application No.: 10/725,720 Confirmation No.: 4318
Filed: December 2, 2003 Art Unit: 2836
For: POWER SUPPLY SYSTEM Examiner: M.R. Wallis

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on June 19, 2007, and is in furtherance of said Notice of Appeal. The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF. This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.02:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 17 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 1-6 and 12-15
2. Claims withdrawn from consideration but not canceled: 16-27
3. Claims pending: 7-11 and 16-27
4. Claims allowed: None
5. Claims rejected: 7-10
6. Claims objected to: 11

C. Claims On Appeal

The claims on appeal are claims 7-10.

IV. STATUS OF AMENDMENTS

A Final Office Action (*Final Office Action*) rejecting the claims of the present application was mailed on April 19, 2007. In response, Appellant did not file an Amendment After Final Rejection, but instead filed a Notice of Appeal, which this brief supports. Accordingly, the claims on appeal are those as rejected in the *Final Office Action*. A listing of the claims on appeal is provided in the "Claims Appendix" section of this brief.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in the independent claim involved in the appeal, referring to the Specification by page and line number and to the Drawings by reference characters, as required by 37 C.F.R. § 41.37. As such, each element of the claims is identified by a reference to the Specification and Drawings, where applicable. However, citation to passages in the Specification and Drawings does not imply that elements recited therein should be read into corresponding claim elements.

According to one claimed embodiment, such as that of independent claim 7, a method for supplying power to an electronic load (*e.g.*, paragraph [0020], figure 4) comprises connecting a plurality of power supplies in parallel (*e.g.*, paragraph [0020], figure 4, step 400), setting, via a power selector circuit, a maximum effective voltage for each of said plurality of power supplies to cascade from a highest effective voltage for a first of said plurality to a lowest effective voltage for a last of said plurality (*e.g.*, paragraph [0020], figure 4, step 401), and interfacing said plurality of power supplies with said electronic load through said power selector circuit (*e.g.*, paragraph [0020], figure 4, step 402).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. First Ground

Claims 7 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 3,600,598 (*Foerster*).

B. Second Ground

Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Foerster* in view of U.S. Patent Publication No. 2003/0095036 (*Wasaki*).

C. Third Ground

Claims 7 and 10 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,760,276 (*Lethellier*) in view of U.S. Patent No. 4,924,170 (*Henze*).

VII. ARGUMENT

Appellant respectfully traverses the outstanding rejections of the pending claims, and requests that the Board reverse these rejections in light of the remarks contained herein. The claims do not stand or fall together, and Appellant presents separate arguments for several claims. Each of the separately argued claims are presented with separate headings and sub-headings in accordance with 37 C.F.R. § 41.37(c)(1)(vii).

A. First Ground (claims 7 and 8)

Claims 7 and 8 are rejected under 35 U.S.C. § 102(b) as being anticipated by *Foerster*. *Final Office Action* at p. 6. Appellant traverses the rejection and asserts that the claims are allowable, at least, for the reasons stated below.

In order to anticipate a claim under 35 U.S.C. § 102, a single reference must teach each and every element of the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). In fact, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). Furthermore, for a reference to be anticipatory, "[its] elements must be arranged as required by the claim." *In re Bond*, 910 F.2d 831 (Fed. Cir. 1990), *cited in* M.P.E.P. § 2131. As described in detail below, Appellant respectfully asserts that *Foerster* does not teach or suggest every element recited in the claims.

Claim 7 recites, in part, "setting, via a power selector circuit, a maximum effective voltage for each of said plurality of power supplies." In contrast, *Foerster* does not indicate that the effective voltage of its power supply modules (PS1'—PS4') is set via a power selector circuit. To aid the Board in better understanding the operational aspects of *Foerster*'s circuit, Appellant points to col. 4, lns 31-36 of *Foerster*, which states that:

> [i]n the event the load L5', for example, supplies more current that is drawn by loads L2' and L6', the excess current, instead of being shunted through a resistor,

> is applied through the switch 32 to the transformer winding 22 for redistribution to one of other levels requiring a current source.

Thus, rather than wasting power through a shunt resistor when a load changes, *Foerster*'s circuit operates to re-distribute that "excess current" to other loads. *See e.g.*, *Foerster* at Figure 2. However, *Foerster*'s redistribution of electrical current due to load changes does not set the voltages of any of power supply modules PS1'—PS4'. *See Foerster* at col. 3, lns. 67—70.

In the *Final Office Action*, the Examiner states that "one should note [that the] cascade of parallel sources of [*Foerster*] is set [to] form a maximum effective voltage (+18v) to a lowest effect voltage (-12v)." *Final Office Action* at p. 3. In response, Appellant asserts that merely arranging power supply modules in a cascaded configuration is not the same as setting the maximum effective voltage of each of those power supply modules via a power selector circuit, as recited in the claim. The Examiner also states that a "selector circuit sets the maximum effective voltage supplied to the load by the translation and redistribution of power levels between loads." *Id.* at p. 4. However, as noted above, *Foerster*'s circuit merely provides a redistribution of electrical current due to load changes. *See Foerster* at col. 3, lns. 67—70. *Foerster*'s redistribution of electrical current in conjunction with a redistribution of loads does not set or change the voltages of power supply modules PS1'—PS4'. *See id.*

Therefore, Appellant respectfully submits that *Foerster* does not teach every element of claim 7. Claim 8 depends from claim 7 and is patentable at least for the same reasons. Accordingly, Appellant respectfully requests that the Board overturn the 35 U.S.C. § 102(b) rejection of record with respect to claims 7 and 8.

B. Second Ground (claim 9)

Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Foerster* in view of *Wasaki*. *Final Office Action* at p. 7. Appellant traverses the rejection and asserts that the claim is allowable, at least, for the reasons stated below.

It is well settled that "[t]he examiner bears the initial burden of factually supporting any *prima facie* case of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." MPEP § 2142. To make a *prima facie* case of obviousness, the Examiner must determine the "scope and content of the prior art," ascertain the "differences between the prior art and the claims at issue," determine "the level of ordinary skill in the pertinent art," and evaluate evidence of secondary considerations. *Graham v. John Deere*, 383 U.S. 1, 17, (1966); *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. ___ (2007); *see also* M.P.E.P. § 2141. When determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. M.P.E.P. § 2141.02(I).

The Supreme Court in *KSR* stated that it is "important [for an examiner] to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the [prior art] elements" in the manner claimed. *KSR Int'l Co. v. Teleflex, Inc.*, No. 04-1350, slip op. at 14 (U.S. April 30, 2007). Indeed, the Court indicated that there should be an "explicit" analysis regarding "whether there was an ***apparent reason*** to combine the known elements ***in the fashion claimed*** by the patent at issue." *Id.* (emphasis added). Further, the Court did not totally reject the use of "teaching, suggestion, or motivation" test as a factor in the obviousness analysis. *Id.* at 14-15.

1. No Apparent Reason to Combine

The rejection of claim 9 should be withdrawn at least because there is no apparent reason for a combination of *Wasaki* with *Foerster*. In support for the combination, the Examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify *Foerster* to include the use of impedance selection to maximize the power output to the load." *Final Office Action* at p. 7. However, *Foerster*'s power supply already operates to maximize the output to its loads. *See Foerster* at Abstract; col. 1, lns. 43-75. Appellant

respectfully asserts that a person of ordinary skill in the art would not have a reason to "add" a power output maximization feature into *Foerster* because *Foerster* already has that feature.

More importantly, contrary to the Examiner's contention, *Wasaki* does not teach an "impedance selection" circuit, but rather it teaches an "impedance matching" circuit. *E.g.*, *Wasaki* at ¶¶ [0060]; Figure 1, element 20. In an attempt to provide some indication of how the "impedance matching" circuit of *Wasaki* could be used to benefit *Foerster*, the Examiner states that "[*Foerster*] teaches a switching system to minimize losses however the further inclusion of selecting or matching the impedance would still provide value to [*Foerster*] by reducing the needed switching of the system of *Foerster*." In response, Appellant respectfully asserts that the impedance matching circuit of *Wasaki*, which is designed for use over power lines—*i.e.*, AC circuits—would not in fact "reduce the needed switching" of the DC power supply system of *Foerster*. *Compare Wasaki* at ¶ [0002] *with Foerster* at col. 1, lns. 6-10.

In sum, neither the applied art nor the knowledge available to a person of ordinary skill in the art suggest the desirability of the combination, and Appellant asserts that there is no apparent reason to combine *Foerster* with *Wasaki*. Accordingly, Appellant respectfully requests that the Board overturn the 35 U.S.C. § 103(a) rejection of record with respect to claim 9 for at least this reason.

2. Lack of All Claimed Elements

As noted above, *Foerster* fails to teach or suggest every element recited in claim 7. The Examiner does not rely upon *Wasaki* as teaching or suggesting these elements, and Appellant asserts that *Wasaki* does not teach or suggest such features. Therefore, the combination of *Foerster* with *Wasaki*, even if proper, fails to teach or suggest all of the elements of independent claim 7. Dependent claim 9 depends from claim 7, thus inheriting all the features of that independent claim. Consequently, the combination of *Foerster* with *Wasaki*, even if proper, also fails to teach or suggest all of the elements of dependent claim 9. Accordingly, Appellant

respectfully requests that the Board overturn the 35 U.S.C. § 103(a) rejection of record with respect to claim 9 for this further reason.

C. Third Ground (claims 7 and 10)

Claims 7 and 10 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lethellier* in view of *Henze*. Appellant traverses the rejection and asserts that the claims are allowable, at least, for the reasons stated below.

1. No Apparent Reason to Combine

The rejection of claims 7 and 10 should be withdrawn because there is no apparent reason for a combination of *Lethellier* with *Henze*. In support for the combination, the Examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention to modify *Lethellier* in view of *Henze* to cascade the plurality of supplies in order of effective voltage in order to supply the ***correct voltage*** to the load." *Final Office Action* at p. 8 (emphasis added). However, Appellant asserts that *Lethellier* already provides correct voltage to a load, as can be immediately seen from the fact that each of *Lethellier*'s loads is directly connected to each of its power supplies. *See Lethellier* at col. 3, lns. 3-12; Figure 2.

In the *Final Office Action*, the Examiner states that "it remains the position of the Office [that] the cascading from high to low of the [power supplies] would have been obvious to one of ordinary skill in the art at the time of the invention in order to arrange the system so the ***correct power*** is supplied to the load." *Final Office Action* at p. 5 (emphasis added). First, Appellant respectfully notes that providing "correct power" is not necessarily the same as providing "correct voltage." *Id.* at p. 8. Second, contrary to the Examiner's assertion, the mere fact that power supplies may be cascaded from high to low voltages does not guarantee or otherwise facilitate the supply of correct power to loads. Furthermore, *Lethellier*'s power supply already provides the "correct power" to its loads. *See Lethellier* at Abstract; col. 3, lns. 3-24. Therefore, the Examiner has failed to establish an apparent reason why a person of ordinary skill in the art would have "added" *Henze* into *Lethellier*.

In sum, neither the applied art nor the knowledge available to a person of ordinary skill in the art suggest the desirability of the combination, and Appellant asserts that there is no apparent reason to combine *Lethellier* with *Henze*. Accordingly, Appellant respectfully requests that the Board overturn the 35 U.S.C. § 103(a) rejection of record with respect to claims 7 and 10 for at least this reason.

2. Lack of All Claimed Elements

Claim 7 recites, in part, "setting, via a power selector circuit, a maximum effective voltage for each of said plurality of power supplies." Appellant has been unable to find any passage of *Lethellier* that indicates that the effective voltage of power supply sets SET 1—SET 3 is set or otherwise controlled in any way. In response to Appellant's remarks, the Examiner states that "[*Lethellier*] points out [that] when a supply is removed or disconnected from the system[,] the other supplies are controlled to supply power to the other loads to provide redundancy. Therefore the loads are in fact controlled." *Final Office Action* at p. 5. First, Appellant respectfully notes that *Lethellier* does not control its loads, but rather it provides a redistribution of electrical current among loads. *Lethellier* at col. 2, lns. 17-21. And, perhaps even more importantly, "controlling a load" is clearly not the same as setting a voltage, much less setting a maximum effective voltage of a plurality of power supplies via a power selector circuit, as recited in the claim. The Examiner does not rely upon *Henze* as meeting these features, and Appellant asserts that *Henze* does not meet such features. Thus, the combination of *Lethellier* with *Henze*, even if proper, does not teach or suggest every element recited in claim 7.

Dependent claim 10 depends from claim 7, thus inheriting all the features of that independent claim. Consequently, the combination of *Lethellier* with *Henze*, even if proper, also fails to teach or suggest all of the elements of dependent claim 10. Accordingly, Appellant respectfully requests that the Board overturn the 35 U.S.C. § 103(a) rejection of record with respect to claims 7 and 10 for this further reason.

CONCLUSION

In view of the above, Appellant requests that the board overturn the outstanding rejections of claims 7-10. Attached hereto are a Claims Appendix, Evidence Appendix, and Related Proceedings Appendix. As noted in the attached Evidence Appendix, no evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted. Also, as noted by the Related Proceedings Appendix, no related proceedings are referenced in II above, and thus no copies of decisions in related proceedings are provided.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: August 15, 2007

Signature: Donna Forbit
(Donna Forbit)

Respectfully submitted,

Roy M. Zeighami

By _____

Jody C. Bishop
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VIII. CLAIMS APPENDIX

7. A method for supplying power to an electronic load comprising:

connecting a plurality of power supplies in parallel;

setting, via a power selector circuit, a maximum effective voltage for each of said plurality of power supplies to cascade from a highest effective voltage for a first of said plurality to a lowest effective voltage for a last of said plurality; and

interfacing said plurality of power supplies with said electronic load through said power selector circuit.

8. The method of claim 7 wherein said interfacing further comprises:

preventing current generated by one of said plurality of power supplies from sinking into another of said plurality.

9. The method of claim 7 wherein said setting further comprises:

selecting impedance values within said power selector circuit to create said maximum effective voltage.

10. The method of claim 7 further comprising:

limiting said maximum effective voltage of one of said plurality of power supplies to a value of a next one of said plurality when said electronic load causes said maximum effective voltage of said one of said plurality to decrease to said maximum effective voltage of said next one of said plurality.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings or copies of decisions in related proceedings are being submitted.